Abstract of the Disclosure

The present invention provides a device having an N type polysilicon gate and a P type polysilicon gate disposed therein, wherein when both gates are simultaneously etched, they are disposed in such a manner that the area of a non-doped polysilicon gate corresponding to a dummy electrode becomes larger than the total area of the N type and P type doped polysilicon gates, thereby causing non-doped polysilicon to become dominant over doped polysilicon, whereby the polysilicon gates are dry-etched.